Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

Cancel claims 2, 3, 9 and 10.

Amend claims 1, 7, 8 and 15.

Add new claims 21-25.

1. (Currently amended) A method of operating a processor comprising:

in a single ~~clock~~ cycle in a parallel hardware-based multithreaded processor, concatenating a first 32-bit word and a second 32-bit word to produce ~~an~~ a 64-bit intermediate result;

shifting the 64-bit intermediate result by a specified shift amount; and

storing the shifted 64-bit intermediate result in a third 32-bit word.

2. (Cancel)

3. (Cancel)

4. (Original) The method of claim 1 wherein shifting comprises right shifting.

5. (Original) The method of claim 4 wherein the specified shift amount is in an operand.

6. (Original) The method of claim 4 wherein the specified shift amount is a value between one and thirty-one.

7. (Currently amended) The method of claim 4 wherein the specified shift amount is a value contained in a lower five bits of the first 32-bit word.

8. (Currently amended) A computer instruction comprising:

in a single ~~clock~~ cycle in a parallel hardware-based multithreaded processor, an instruction to concatenate a first 32-bit word and a second 32-bit word to produce ~~an~~ a 64-bit intermediate result;

shift the 64-bit intermediate result by a specified amount; and

store the shifted 64-bit intermediate result in a third 32-bit word.

9. (Cancel)

10. (Cancel)

11. (Original) The instruction of claim 8 wherein shifting comprises right shifting.

12. (Original) The instruction of claim 11 wherein the specified amount is in an operand.

13. (Original) The instruction of claim 11 wherein the specified amount is a value between one and thirty-one.

14. (Original) The instruction of claim 11 wherein the specified amount is a value contained in a lower five bits of the first word.

15. (Currently amended) A method comprising:

in a single cycle in a parallel hardware-based multithreaded processor, concatenating a first 32-bit operand and a second 32-bit operand to produce a 64-bit concatenation result;

right shifting the 64-bit concatenation result by a specified amount; and

storing a lower 32 bits of the right shifted 64-bit concatenation result in a 32-bit destination register.

16. (Previously presented) The method of claim 15 in which the first 32-bit operand is a context-relative register name.

17. (Previously presented) The method of claim 15 in which the second 32-bit operand is a context-relative register name.

18. (Previously presented) The method of claim 15 in which the specified amount is a value from 1 to 31.

19. (Previously presented) The method of claim 15 in which the destination register is an absolute register name.

20. (Previously presented) The method of claim 15 in which the destination register is a context-relative register name.

Add the following new claims 21-25.

21. (New) A hardware-based multithreaded processor comprising:

a plurality of microengines, each of the microengines comprising:

a control store;

controller logic;

context event switching logic; and

an execution box data path including an arithmetic logic unit (ALU) and a general purpose register set, the ALU performing functions in response to instructions, one of the

instructions causing the ALU to load a destination register with a 32-bit long word formed by concatenating a first operand and a second operand to form a 64-bit quantity, shifting the 64-bit quantity by a specified amount, and storing a lower 32-bits of the 64-bit quantity.

22. (New) The processor of claim 21 in which the first operand is a context-relative 32-bit register.

23. (New) The processor of claim 21 in which the second operand is a context-relative 32-bit register.

24. (New) The processor of claim 21 in which the destination register is a context-relative 32-bit register.

25. (New) The processor of claim 21 in which the specified amount is a value representing a right shift of values from 1 to 31.